POWER SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING SAME

TECHNICAL FIELD

[0001] The present invention relates to a power semiconductor device such as a silicon carbide semiconductor device.

BACKGROUND ART

[0002] In a power semiconductor device constituted by a power vertical metal oxide semiconductor field effect transistor (MOSFET) described in Patent Document 1 and a diode, the diode is disposed in at least one line in an adjacent region to a peripheral edge part of a cell region of the MOSFET, that is, a gate pad portion as shown in FIGS. **1** and **2** of the same Document. Each diode absorbs a hole injected in a forward bias from a P well and a P base into an N-type semiconductor layer on a drain side as shown in FIG. **2** of the same Document when the MOSFET is switched from an ON state to an OFF state. For this reason, the structure disclosed in the same Document can prevent a parasitic transistor shown in FIG. **3** of the same Document from being turned ON when the MOSFET is switched from the forward bias to a reverse bias.

[0003] With the structure in the same Document, the P base to be the P well of the MOSFET is electrically connected to a source electrode through a back gate as shown in FIG. **2**.

Prior Art Document

Patent Document

[0004] Patent Document 1: Japanese Patent Application Laid-Open No. 5-198816 (FIGS. **1** to **3**)

SUMMARY OF THE INVENTION

Problem to be Solved by the Invention

[0005] Problems to be solved by the present invention will be described below with reference to FIG. **2** of the Patent Document 1.

[0006] When the MOSFET of the power semiconductor device described in the Patent Document 1 is switched from an ON state to an OFF state, a drain voltage of the MOSFET, that is, a voltage of a drain electrode is suddenly raised and reaches approximately several hundreds V in some cases. By the rise in the drain voltage, a displacement current is generated on a drain electrode side and a source electrode side through a depletion layer capacitance formed between a P well and an N-drain layer when the OFF state is brought. The displacement current is also generated in a diode as well as the P well of the MOSFET in the P well or a place where a P-type region is provided in the N-drain layer in the same manner as the P well.

[0007] The displacement current generated on the drain electrode side exactly flows to the drain electrode, and the displacement current generated on the source electrode side flows to the source electrode via the P well or the P-type region.

[0008] In the case of the power semiconductor device described in the Patent Document 1, a source electrode and a field plate are electrically connected to each other as described in the description of the related art. For this reason, in a section shown in FIG. **2**(C), for example, a displacement current flowing into a P well provided under a gate pad flows toward a contact hole connected to the field plate in an MOSFET cell direction in the P well provided under the gate pad and flows into the source electrode through the field plate.

[0009] An area of the P well provided under the gate pad is much larger than areas of a P well of an MOSFET cell and a P well of a diode cell. When the displacement current flows to the P well provided under the gate pad, therefore, a voltage which cannot be disregarded is generated in the P well because the P well itself having a large area and a contact hole have resistances having great resistance values to some degree. As a result, a comparatively high electric potential is generated in a position in a P well having a great distance in a planar direction from a place (a contact hole) in which the P well is electrically connected to a source electrode (which is usually connected to a ground potential) through the field plate.

[0010] This electric potential is raised when the displacement current is increased, and is raised when a fluctuation dV/dt of a drain voltage V to a time t is increased.

[0011] In the power semiconductor device including the MOSFET, a high voltage is generated in the P well as described above when the voltage of the gate electrode approximates to the vicinity of 0 V immediately after the MOSFET is switched from the ON state to the OFF state in a place where a gate insulating film of the MOSFET is interposed between the P well and the gate electrode, and the gate insulating film is broken by a high electric field due to the high voltage in some cases.

[0012] The present invention has been made to solve the problem and has an object to provide a power semiconductor device including an MOSFET to be switched at a high speed which can suppress an occurrence of a dielectric breakdown between a gate electrode and a source electrode in the switching and has a high reliability, and a method of manufacturing the same.

Means for Solving the Problem

[0013] A power semiconductor device according to the present invention includes a semiconductor substrate of a first conductivity type, a drift layer of the first conductivity type which is formed on a first main surface of the semiconductor substrate, a plurality of first well regions of a second conductivity type which is formed in a part of a surface layer of the drift layer, a source region of the first conductivity type which is formed in a part of a surface layer of each of the first well regions, a second well region of the second conductivity type which is formed apart from the first well regions to surround the first well regions, a gate insulating film formed on the first well regions and the source region, and at the first well region side on the second well region, a field insulating film formed on an opposite side to the first well region side on the second well region and having a greater film thickness than the gate insulating film, a gate electrode formed on the field insulating film and the gate insulating film, a source pad for electrically connecting the first well region and the second well region through a source contact hole formed on the first well region to penetrate the gate insulating film and a second well contact hole formed on the second well region to penetrate the field insulating film, a gate pad connected electrically to the gate electrode, and a drain electrode provided on a second main surface of the semiconductor substrate.

[0014] Moreover, a method of manufacturing a power semiconductor device according to the present invention includes the steps of forming a drift layer of a first conductivity type on a first main surface of a semiconductor substrate